

ARM Holdings: Portfolio Report



Introduction

Arm Holdings is a leading semiconductor company that designs microprocessors, physical intellectual property (IP) and related technology and software. Headquartered in Cambridgeshire, U.K., the company develops and licenses technology that forms the core of many digital electronic devices such as smartphones, servers and sensor-based products. ^[1]

ARM's strength is its patent assets. The company makes significant investment in its research and development (R&D) efforts to build mobile processor core and system designs, and licenses or sells them to electronics and system companies. ^[2]

In 2016, SoftBank Group took over Arm Holdings to address the Internet of Things (IoT) space. As a part of its IoT strategy, Arm has made several acquisitions, the most recent one being the acquisition of Treasure Data. This comes as a part of the company's plan to launch a new connectivity and data management software-as-a-service (SaaS) platform. [3]

Being a company that relies heavily on its intellectual assets, Arm boasts of an interesting patent and technology portfolio. This report analyses the patent assets held by Arm Holdings and provides insights into various aspects of the overall portfolio.

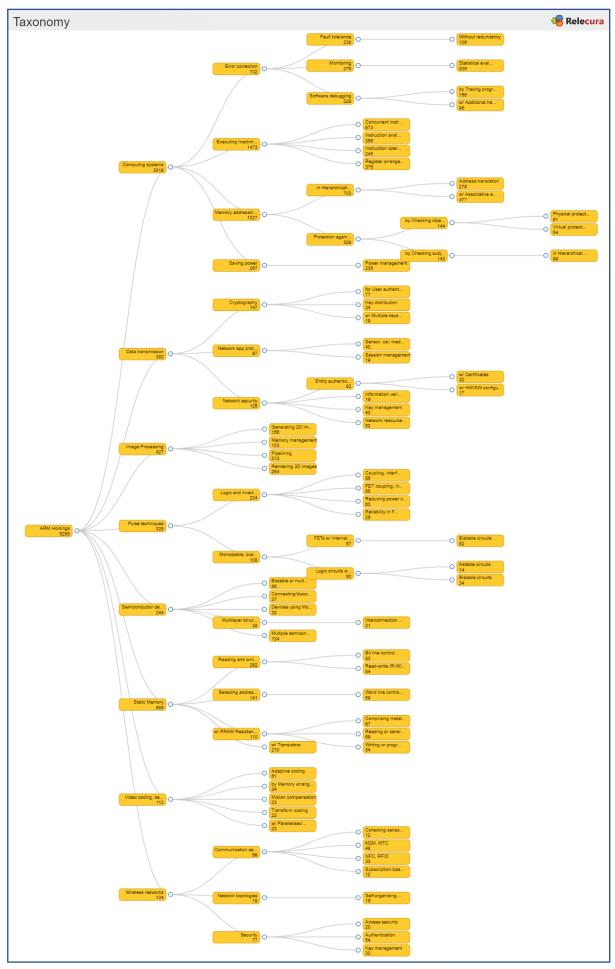
Contents

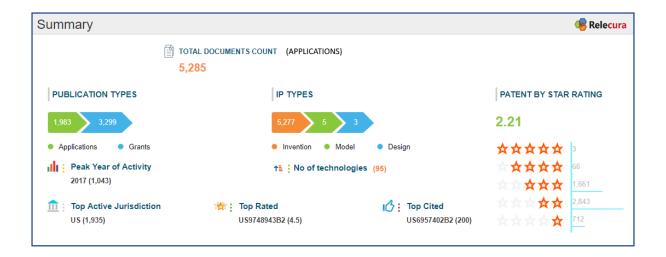
- Taxonomy
- Summary
- Portfolio trends
- Key geographies
- Key technologies
- Analysis of key technologies
- Key sub-technologies

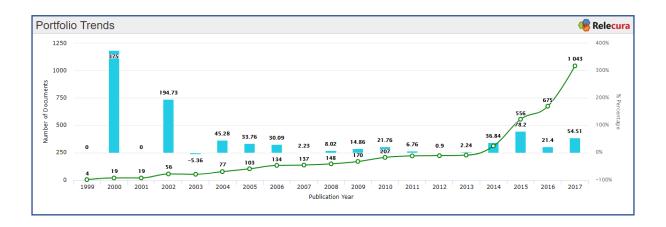
- Evolution of key sub-technologies
- Patent quality
- Key patents
- Top forward citing (FC) assignees
- Technology focus of FC assignees
- Topic map Concepts

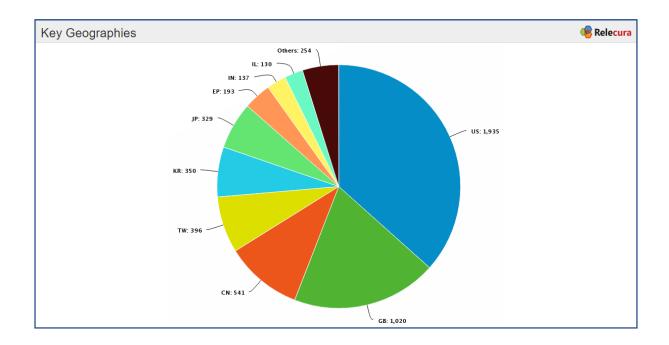
Sources

- 1. Arm Holdings (Wikipedia.org)
- 2. Arm Holdings Annual Strategic Report (Annual reports.com)
- 3. <u>Sealing Treasure Data buy, Arm launches Pelion IoT Platform to manage data on any device</u> (siliconangle.com)





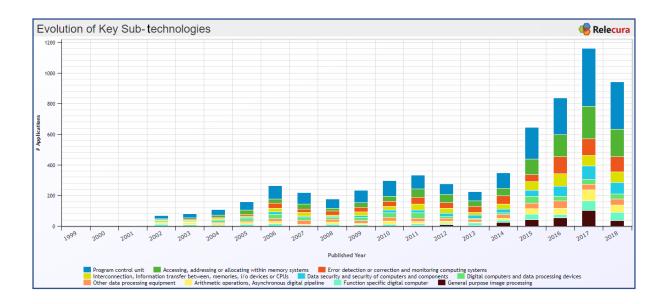


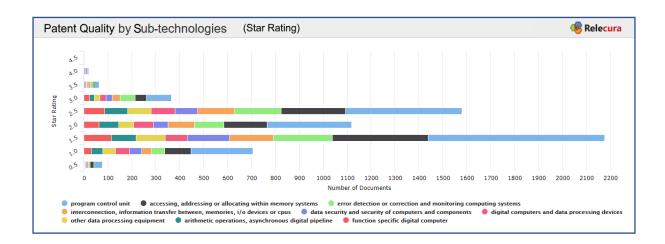


Key Technologies			Relecura
	Technologies	# Applications	
	Digital Data Processing	3812	
	Static Memory	584	
	Image Data Processing	427	
	Data Transmission	380	
	Pulse Techniques	323	
	Electric Elements - Semiconductor Devices	244	
	Measurement - Electric & Magnetic Variables	204	
	Pictorial Communication	155	
	Displays (Circuits)	133	

Technologies	Applications	Grants	Sub Technologies	Geographies
digital data processing	1323	2491	program control unit (2000), accessing, addressing or allocating within memory systems (1034), error detection or correction and monitoring computing systems (703), interconnection, information transfer between, memories, i/o devices or cpus (536), data security and security of computers and components (420)	US (1374) , GB (689) CN (411) , JP (278) , KR (235)
static memory	172	412	reading and writing of data to an memory (262), memories using electric or magnetic storage elements (259), selecting address in memory (141), details of semiconductor memories (124), testing and repairing memories (121)	US (260) , TW (118) , KR (55) , GB (50) , CM (41)
image data processing	158	269	general purpose image processing (277) , rendering 3d images (264) , generating 2d images (156) , circuits for display devices (98) , architecture of display device (68)	US (154) , GB (138) , CN (62) , KR (32) , JF (25)
data transmission	159	221	cryptographics for secret digital communication (147), data security and security of computers and components (131), architecture for network security (125), arrangements, apparatus, circuits or systems for digital transmission (118), program control unit (103)	US (161) , GB (83) , CN (46) , KR (32) , JF (16)
pulse techniques	88	236	logic and inverting circuits (203), monostable, bistable or multistable circuits (108), electronic switching and gating (54), other data processing equipment (51), manipulating electric pulses (47)	US (131), TW (71), GB (38), KR (25), CN (23)

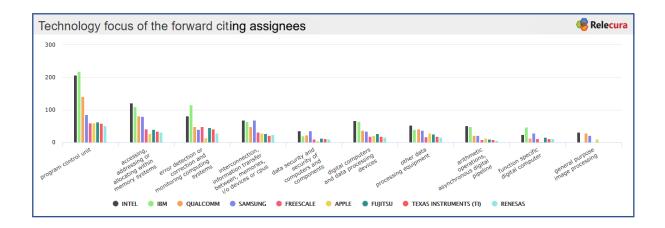
Key Sub-technologies	Relecura 🕏
Sub-technologies	# Applications
Program Control Unit	1995
Accessing, Addressing or Allocating Within Memory Systems	1033
Error Detection or Correction and Monitoring Computing Systems	701
Interconnection, Information Transfer Between, Memories, I/O	536
Devices or CPUs Data Security and Security of Computers And Components	420
Digital Computers and Data Processing Devices	367
Other Data Processing Equipment	365
Arithmetic Operations, Asynchronous Digital Pipeline	356
Function Specific Digital Computer	324

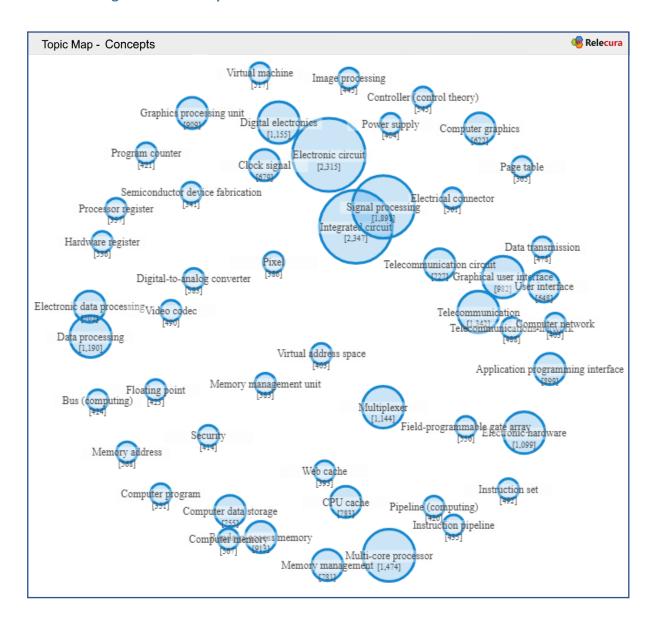






Top Forward Citing Assignees	Relecura
FC Assignee	# Applications
INTEL	484
IBM	473
QUALCOMM	364
SAMSUNG	341
FREESCALE	177
APPLE	160
FUJITSU	157
TEXAS INSTRUMENTS	144
RENESAS	126





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About Relecura

Relecura is a full-stack cognitive cloud platform that provides custom intelligence and reports on patent portfolios, technologies and companies. It does this by capturing and organizing the knowledge from various document repositories (patents, scientific literature) and subject matter experts in a flexible and collaborative manner, into a knowledge-base.

Relecura offers IP analytics tools and a custom enterprise platform to corporations, law firms, IP services firms, R&D organizations and academic institutions. The enterprise platform integrates the discovery and analysis of public documents with internal company documents. Relecura also has an API to help create custom tools for IP and business intelligence.



ARM Holdings
Competitive Comparison and Growth Trends

September 2018



Introduction

Relecura's Taxonomy delivers comparative insights on patents across multiple company portfolios or different time periods – all in the matter of a few steps. This makes it particularly suited to generate competitive insights and growth trends for different sub-categories within the technology domain of interest.

We have created a few such analytics snapshots comparing the patent assets held by ARM Holdings with its competitors in the CPU and GPU space (Table 1), as well as comparing ARM's portfolio to those of a couple of large players, i.e. Intel and Qualcomm (Table 2).

Table 3 once again compares ARM's portfolio in its various categories to those of its competitors in the GPU and CPU space, the difference being that we focus only on the high-quality patents in each of the portfolios.

Finally, in Table 4 we look at growth trends year-wise in each of the ARM's portfolio categories in the 2012-2017 period, and compare them to the trends in all of the patents published year-wise in the same period.



Table 1. ARM Holdings vs. Competitors (GPU/CPU)

			Number of Applications given for nodes	coded				PU	GPI	U
			Brenton Brentol House			ARM	AMD	MIPS	Imagination	
	T		Fault tolerance	Without redundancy		106	25	MIPS	Imagination 11	nVidia 47
								2		
		Error correction	Monitoring	Statistical evaluation of computer activity		205	59	3		37
			Software debugging	by Tracing program execution		155	19	0	8	10
				w/ Additional harware		96	14	0	3	6
			Concurrent instruction execution, e.g.			973	579	217	242	527
			pipeline, look ahead							
			Instruction analysis, e.g. decoding,			356	93	38	52	44
		Executing machine instructions	instruction word fields						39	55
	Computing systems		Instruction operation extension or			245	110	21	39	55
			modification				_	_		
			Register arrangements		I	375	96	62		93
			L		Physical protection, e.g. cell, word, block	91	21	0	0	7
			Protection against unauthorised memory	by Checking object accessibility	Virtual protection, e.g. for virtual blocks or	54	18	1	0	1
		Memory addressing, allocation	use		segments before a translation mechanism		_	_		
				by Checking subject access rights	in Hierarchical protection system	89	44	2	2	0
			in Hierarchically structured memory systems	Address translation		278 477	268 541	15 63		141 204
				W/ Associative addressing						
		Saving power	Power management			235	447	6		250
		0	Key distribution			34	16	2	4	11
		Cryptography	for User authentication			77	30	0	3	16
		<u> </u>	w/ Multiple keys, algorithms	-		19	4	0	2	0
		Network app protocols	Sensor, car, medical networks	-		40	2		0	1
	Data transmission		Session management	10-11-1-	1	19	3	0		21
			Entity authentication	w/ Certificates		32	0	0	0	0
		Natural accepts		w/ HW/SW configuration	I	17	1	0	3	0
		Network security	Information verification	1		19 43	9	0	3	0
			Key management				11	-	3	2
		Cti 2D I	Network resource access	J		52	15	0	0	3
		Generating 2D Images				156	91	0		333
	Image Processing	Memory management				123	149	0		321
		Pipelining				213	268	1		622
		Rendering 3D images		1		264	323	0	533	1064
			Coupling, interface arrangements			86	52	0		28
	Pulse techniques	Logic and inverting circuits	FET coupling, interface arrangements			65	35	0		11
		-	Reducing power consumption			63	30	0	0	10
			Reliability in FET circuits		1	25	25	0	0	1
			FETs w/ internal, external positive feedback			52	24	0		51
ARM Holdings		Monostable, bistable or multistable circuits	Logic circuits w/ internal, external positive feedback	Astable circuits Bistable circuits		14 34	10	0		11
		manufacture of the second	reedback	Bistable circuits			12			18
vs Competitors		Bistable or multistable switching devices				86 37	744	0	0	164
		Connecting/disconnecting semiconductor				37	744	0	0	104
		bodies				22	0			
	Semiconductor devices	Devices using Mott metal-insulator				32	0	0	0	0
	Semiconductor devices	transition, e.g. field effect transistors Multilayer structure of conductive and		1		31	36	0	0	
			Interconnection layout	J		134	718	0	0	27
		Multiple semiconductor or solid state devices components formed on a common				134	/18	ľ	0	21
		substrate		1		83	13			25
			Bit line control circuits, e.g. drivers,			03	13	ľ	0	23
		I	boosters, pull-up circuits, pull-down circuits							
		Reading and writing of data to an memory	precharging circuits, equalising circu	1						
		nessing and writing or data to an memory	Read-write (R-W) timing or clocking circuits;	†		84	41	0	0	28
		I	Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators	1		34	***	ľ	ľ	20
			or management							
		H	Word line control circuits, e.g. drivers,	1		59	34	0	0	6
	Static Memory	Selecting address in memory	boosters, pull-up circuits, pull-down circuits,			33	-	ľ	ľ	ľ
		second address minemory	precharging circuits, for word lines	1						
			Comprising metal oxide memory material,	1		67	3	0	0	0
i e				I		,	ľ	ľ	ľ	ľ
			e a nerovskites				1	0	0	0
		w/ RRAM Resistance random access memory	e.g. perovskites			69	1		I.A.	1*
		w/ RRAM Resistance random access memory elements	e.g. perovskites Reading or sensing circuits or methods	-		69	11	0	n	0
		w/ RRAM Resistance random access memory elements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods			69 84	11		0	0
		CHETTO	e.g. perovskites Reading or sensing circuits or methods			84				Ů
		w/ Transistors	e.g. perovskites Reading or sensing circuits or methods			84 210	115		0	94
		w/ Transistors Adaptive coding	e.g. perovskites Reading or sensing circuits or methods			210 61	115 133	0	0 86	94
		w/Transistors Adaptive coding Motion compensation	e.g. perovskites Reading or sensing circuits or methods			210 61 23	115 133 58	0 0 0	0 86 52	94 150 50
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding	e.g. perovskites Reading or sensing circuits or methods			210 61	115 133 58 63	0 0 0 0	0 86 52 47	94 150 50 104
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements	e.g. perovskites Reading or sensing circuits or methods			210 61 23 23	115 133 58	0 0 0	0 86 52 47	94 150 50 104 52
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding	e.g. perovskites Reading or sensing circuits or methods			210 61 23 23 24	115 133 58 63 42	0 0 0 0	0 86 52 47	94 150 50 104
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods			210 61 23 23 24 23	115 133 58 63 42	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 86 52 47 42 25	94 150 50 104 52
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding My Memory arrangements w/ Parallelised computational arrangements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods Collecting sensor information			210 61 23 23 24 23	115 133 58 63 42	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 86 52 47 42 25	94 150 50 104 52
	Video coding, decoding	w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods Writing or programming circuits or methods Collecting sensor information MAM, MTC			210 61 23 23 24 23 12 48	115 133 58 63 42	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 86 52 47 42 25 0 3	94 150 50 104 52
		w/ Transistors Adaptive coding Motion compensation Transform coding My Memory arrangements w/ Parallelised computational arrangements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods. Collecting sensor information MZM, MTC NCC, RFID			210 61 23 23 24 23 12 48 30	115 133 58 63 42	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 86 52 47 42 25	94 150 50 104 52
	Video coding, decoding Wireless networks	w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements w/ Parallelised computational arrangements Communication services	e.g. perovikites Reading or sensing circuits or methods Writing or programming circuits or methods Writing or programming circuits or methods Collecting sensor information MZM, MTC NFC, RFID Subscription-based services			210 61 23 23 24 23 12 48 30	115 133 58 63 42	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 86 52 47 42 25 0 3	94 150 50 104 52
		w/ Transistors Adaptive coding Motion compensation Transform coding My Memory arrangements w/ Parallelised computational arrangements	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods Writing or programming circuits or methods Collecting sensor information MZM, MTC NPC, RFID Subscription-based services Self-organising networks			210 61 23 23 24 23 12 48 30 12 16	115 133 58 63 42	0 0 0 0 0 0 0 0	0 86 52 47 42 25 0 3 0 0	94 150 50 104 52
		w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements w/ Parallelised computational arrangements Communication services Network topologies	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods Writing or programming circuits or methods Collecting sensor information MZM, MTC NPC, RFID Subscription-based services Self-organising networks Access security			210 61 23 23 24 23 12 48 30 12 16 20	115 133 58 63 42	0 0 0 0 0 0 0 0 0	0 86 52 47 42 25 0 3 0 0 7	94 150 50 104 52 63 0 6 7 9 3 3
		w/ Transistors Adaptive coding Motion compensation Transform coding by Memory arrangements w/ Parallelised computational arrangements Communication services	e.g. perovskites Reading or sensing circuits or methods Writing or programming circuits or methods Writing or programming circuits or methods Collecting sensor information MZM, MTC NPC, RFID Subscription-based services Self-organising networks			210 61 23 23 24 23 12 48 30 12 16	115 133 58 63 42	0 0 0 0 0 0 0 0	0 86 52 47 42 25 0 3 0 0 7	94 150 50 104 52



Table 2. ARM Holdings vs. Large Players (Intel, Qualcomm)

Number of Applications given for nodes coded		ARM	Intel	Qualcomm
Fault tolerance Without redundancy	-	106 205	654 754	161 239
Error correction Monitoring Statistical evaluation of computer activity	Ey .	203	754	237
Software debugging by Tracing program execution		155	175	20
w/ Additional harware		96	132	57
Concurrent instruction execution, e.g. pipeline, look ahead		973	3938	1353
Instruction analysis, e.g. decoding,		356	1772	265
Executing machine instructions Instruction word fields				
Instruction operation extension or		245	758	182
Computing systems modification Register arrangements		375	1377	284
register arangements		91	232	28
	Physical protection, e.g. cell, word, block			
Protection against unauthorised memory by Checking object accessibility	Virtual protection, e.g. for virtual blocks	54	251	36
Memory addressing, allocation use	or segments before a translation mechanism			
by Checking subject access rights	in Hierarchical protection system	89	139	22
in Hierarchically structured memory Address translation		278	1271	482
systems w/ Associative addressing		477	3319	888
Saving power Power management Key distribution		235 34	4126 1045	1993 1063
Cryptography For User authentication		77	1669	1192
w/ Multiple keys, algorithms		19	415	230
Network app protocols Sensor, car, medical networks		40 19	546 302	609 766
Data transmission Session management w/ Certificates		32	302	302
entity authentication w/ HW/SW configuration		17	249	179
Network security Information verification		19	363	557
Key management		43 52	666 1009	1084 869
Network resource access Generating 2D Images		156	496	432
Memory management		123	706	317
Pipelining		213	1026	533
Rendering 3D images		264	1090	755 388
Coupling, interface arrangements FET coupling, interface arrangements		86 65	521 227	260
Logic and inverting circuits Reducing power consumption		63	172	237
Pulse techniques Reliability in FET circuits	_	25	48	92
FETs w/ internal, external positive feedback Monostable, bistable or multistable feedback Bistable circuits		52	152	318
circuits Logic circuits w/ internal external Actable circuits		14	102	109
ARM Holdings vs Competitors positive feedback Bistable circuits		34	106	182
Bistable or multistable switching devices		86	282	23
Connecting/disconnecting semiconductor		37	5833	2428
bodies		-		
Devices using Mott metal-insulator		32	5	0
Semiconductor devices transition, e.g. field effect transistors Multilayer structure of conductive and		31	498	465
insulating layers		31	450	400
Multiple semiconductor or solid state		134	3113	2056
devices components formed on a				
common substrate Bit line control circuits, e.g. drivers,		83	160	240
boosters, pull-up circuits, pull-down		-		
Reading and writing of data to an				
memory Read-write (R-W) timing or clocking		84	402	313
kead-write (k- w) timing or clocking circuits, Read-write (R-W) control signal		34	+02	515
generators or management				
Word line control circuits, e.g. drivers,		59	97	194
Static Memory Selecting address in memory circuits, precharging circuits, for word				
lines				
Comprising metal oxide memory		67	56	6
w/ RRAM Resistance random access material, e.g. perovskites		60	100	60
memory elements Reading or sensing circuits or methods Writing or programming circuits or		69 84	199 263	68
methods				
w/ Transistors		210	1153	917
Adaptive coding Metion compensation		61 23	1013 462	6503 2655
Motion compensation Transform coding		23	477	2780
		24	153	497
by Memory arrangements		23	124	534
by Memory arrangements w/ Parallelised computational				_
by Memory arrangements w/ Parallelised computational arrangements		12	74	1112
by Memory arrangements w/ Parallelised computational arrangements Collecting sensor information		12 48	74 2207	112 1281
by Memory arrangements w/ Parallelised computational arrangements Collecting sensor information M2M, MTC NFC, RFID		48 30	2207 1306	1281 1030
by Memory arrangements w/ Parallelised computational arrangements Collecting sensor information MZM, MTC NFC, RFID Subscription-based services		48 30 12	2207 1306 147	1281 1030 242
by Memory arrangements w/ Parallelised computational arrangements Collecting sensor information MZM, MTC NFC, RFID Subscription-based services Network topologies Self-organising networks		48 30 12 16	2207 1306 147 913	1281 1030 242 2763
by Memory arrangements w/ Parallelised computational arrangements Collecting sensor information MZM, MTC NFC, RFID Subscription-based services		48 30 12	2207 1306 147	1281 1030 242



Table 3. ARM Holdings vs. Competitors (GPU/CPU) – High-quality Patents

We have devised a proprietary patent quality rating that ranks each patent out of five, which we call the 'Relecura Star Rating' of the patent. It is a composite metric based on the findings of studies to determine the characteristics of valuable patents. Patents which score three or more based on this ranking are deemed to be of high-quality.

We have restricted the patents of various companies show below to those with a "Relecura Star Rating" of three or more.

		Number of .	Applications given for nodes coded				C	PU	GI	PU U
						ARM	AMD	MIPS	Imagination	nVidia
			Fault tolerance	Without redundancy		5	3	0	0	7
		Error correction	Monitoring	Statistical evaluation of computer activity		33	3	0	0	4
			Software debugging	by Tracing program execution w/ Additional harware		34 17	1	0	0	0
			Concurrent instruction execution, e.g.	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	J	90	38	27	4	76
Computin			pipeline, look ahead Instruction analysis, e.g. decoding,			29	1	4	1	3
	Computing systems	Executing machine instructions	Instruction word fields Instruction operation extension or	-		23	9	5	0	7
			modification			42			0	15
			Register arrangements		Physical protection, e.g. cell, word, block	42	2	8	0	15
			Protection against unauthorised memory	by Checking object accessibility	Virtual protection, e.g. for virtual blocks or	0	2	0	0	0
			use	by checking object accessionity	segments before a translation mechanism	ľ	1	ľ	ľ	ľ
		Memory addressing, allocation	[·	by Checking subject access rights	in Hierarchical protection system	7	1	1	0	0
			in Hierarchically structured memory	Address translation	, , , , , , , , , , , , , , , , , , , ,	16	26	3	0	25
			systems	w/ Associative addressing		43	39	4	3	29
		Saving power	Power management		•	24	73	0	1	42
			Key distribution			4	1	0	0	1
		Cryptography	for User authentication			7	0	0	0	4
			w/ Multiple keys, algorithms			0	0	0	0	0
		Network and protocols	Sensor, car, medical networks			6	0	0	0	0
	Data transmission	Network app protocols	Session management		_	1	0	0	0	2
	Data (rangiliissiuli		Entity authentication	w/ Certificates		5	0	0	0	0
			Entity authentication	w/ HW/SW configuration		2	0	0	0	0
		Network security	Information verification		=	0	1	0	0	1
1			Key management			6	1	0	0	2
			Network resource access			4	0	0	0	0
		Generating 2D Images				36	10	0	12	59
	Image Processing	Memory management				14	10	0	16	40
	image Processing	Pipelining				23	25	0	12	89
		Rendering 3D images		_		36	30	0	56	177
		Logic and inverting circuits	Coupling, interface arrangements			3	2	0	0	1
	Pulse techniques		FET coupling, interface arrangements			1	2	0	0	0
			Reducing power consumption			5	1	0	0	0
			Reliability in FET circuits			2	0	0	0	0
		Monostable, bistable or multistable	FETs w/ internal, external positive	Bistable circuits		1	1	0	0	1
ARM Holdings vs		circuits	Logic circuits w/ internal, external positive			2	0	0	0	4
Competitors (High			feedback	Bistable circuits		0	0	0	0	0
Quality Patents)		Bistable or multistable switching devices				9	0	0	0	0
		Connecting/disconnecting semiconductor				0	47	0	0	9
		bodies								_
	L	Devices using Mott metal-insulator				1	0	0	0	0
	Semiconductor devices	transition, e.g. field effect transistors Multilayer structure of conductive and		1			-	_	0	0
			Interconnection layout			1	22	0	0	0
		Multiple semiconductor or solid state devices components formed on a common				2	22	ľ	ľ	2
		substrate								
		substrate	Bit line control circuits, e.g. drivers,	1		2	0	0	0	2
			boosters, pull-up circuits, pull-down			-			ľ	1
			circuits, precharging circuits, equalising							
		Reading and writing of data to an memory	circu							
			Read-write (R-W) timing or clocking	1		4	6	0	0	1
			circuits; Read-write (R-W) control signal							
			generators or management							
1			Word line control circuits, e.g. drivers,	1		2	1	0	0	1
	Static Memory	Selecting address in memory	boosters, pull-up circuits, pull-down							
		ocicoung address in memory	circuits, precharging circuits, for word lines							
			Comprising metal oxide memory material,			10	1	0	0	0
1		w/ RRAM Resistance random access	e.g. perovskites							
		memory elements	Reading or sensing circuits or methods			12	0	0	0	0
		,	Writing or programming circuits or			14	0	0	0	0
			methods					-		\perp
		w/ Transistors				6	10	0	0	3
1		Adaptive coding				5	17	0	6	15
		Motion compensation				0	4	0	2	5
1	Video coding, decoding	Transform coding	1			0	13	0	5	11
1		by Memory arrangements				0	8	0	5	9
		w/ Parallelised computational				0	7	0	3	6
		arrangements	0.11.11	1		_		-		
			Collecting sensor information	-		1	0	0	0	0
		Communication services	M2M, MTC	-		3	0	0	0	0
			NFC, RFID	-		2	0	0	0	0
	Wireless networks		Subscription-based services			1	0	0	0	1
		Network topologies	Self-organising networks			2	0	0	1	1
1			Access security	4		2	0	0	0	0
1		Security	Authentication			9	0	0	0	1
			Key management	1		2	0	0	0	0



Table 4. ARM Holdings vs. Overall – Year-wise Comparison of Patents Published

Part			Number	of Applications given for nodes coded						Overall							ARM			
## 18							2012	2013	2014	2015	2016	2017	Overall	ARM	2012	2013	2014	2015	2016	2017
 Materials and the properties of the				Fault tolerance	Without redundancy		_								6	7				
# 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1							2666	_	_		_	_	-	-1	24	21	27	16	58	51
Monthsofunce Mont			Error correction				210	_	_	524	_	_	_		21	_	_	12	20	_
 1. Path in the standard st				Software debugging				-	-	-			/	~		-				-
 14 A TOUR STANDAM PROMOTOR STANDAM PROMOTOR				Concurrent instruction execution,	w/ Additional harware		-	_	_	_	_	_	\sim	\sim	_	_	9	8	37	-
Part				e.g. pipeline, look shead			-	_	_		_	_		$\overline{}$		_	_	_	_	205
Part			Executing machine instructions	instruction word fields			411	701	828	968	1144	1369		\sim	53	51	35	44	70	66
Mathematical Registration		Computing systems	•	modification operation extension or			373	477	568	573	652	758	/	$\overline{}$	38	34	15	41	50	55
Mathematical Part		computing systems					535	825	836	906	1043	1271	/		56	53	47	85	71	82
Mathematical Mat							193	216	267	329	329	370	/		6	3	5	18	22	37
Part				Protection against unauthorised	by Checking object accessibility		116	146	153	175	185	183	_	1	17	12	3	9	9	3
Mathematical Personal Person			Memory addressing, allocation	memory use	by Charking subject access rights		91	112	122	120	125	122	_	\ \/	15	11	6	18	9	19
Mariting			,				_	_	_	_	_	_			_	_			-	-
Management Man				in Hierarchically structured memory systems			-	-	_	_	_	-	_			-		57	"	/0
Part				,	w/ Associative addressing								_	$\overline{}$	-			90		
No. 10. Section Sect			Saving power	Power management			4711	5782	6909	7166	7877			~	30	28	14	39	49	29
Manife the properties Mani				Key distribution			5246	5561	6101	6235	7206	9164	_/	$ \sim $	2	4	5	2	13	18
Manual Protection			Cryptography	for User authentication			10561	10588	10798	10830	11736	13235	_/		1	8	13	15	26	28
Marten Age protection				w/ Multiple keys, algorithms			1198	1185	1288	1561	1822	2556		/	0	0	3	5	5	12
Marten Age protection				Sensor, car, medical networks	1		3129	3539	4516	6302	8579	12812			0	0	0	7	19	16
Marchisou			Network app protocols				-	_	_	_	_	_	_		0	0	1	3	6	6
Many Many Many Many Many Many Many Many		Data transmission			w/ Certificates	1	-	_	_		_	_	_	_	0	3		5	20	12
Hand the foliage of the properties of the proper				Entity authentication	-,								_		_	-		Ĭ.		12
Manual					w/ HW/SW configuration]	-	_	_	_	_	_	/,		0	0	0	4	-	5
Pulse (1988) (1998) (19			Network security				-	_	_	_	_	_	/		0	0	1	5	_	8
Many Processing				Key management			2247	2386	2789	3298	4432	5157	/		0	0	3	11	20	22
Refuse Processing Pro				Network resource access			4982	5659	7005	8209	10125	10728	/		0	1	5	18	25	24
Mag-Pricestring Papeling Pa			Generating 2D Images		•		5577	6549	7765	8713	10325	10794	/		18	17	47	46	48	46
Magning Pipeling Pipeling Reading (3) magning Reading (3) magning (3			Memory management				597	707	1093	1194	1432	1489	_		6	3	23	36	50	53
Residency (a) images (a) supplies a residency (a) supplies (a							996	1130	1560	1838	2200	2528	_	~	23	11	33	63	59	96
The Pulle stationages in the stationage				-					-					_			-	-	-	00
Heat the pulse of meritang coults in extension (and in the pulse of meritang coults in extension (and in the pulse) (and in the	-		Kendering 3D images		1		-	_	_	_	_	_	_	~		_	_	"	70	70
Reference of the conting or conting of the conting							-	_	_	_	_	_	/~	~ \	2.7	12	-	20	10	10
Maching power comunity of the control of the cont	Trends							884		811			\sim	V \	-	8		13	9	7
Part International Control Section Part Par				Reducing power consumption			411	450	493	486	596	554	~	$\overline{}$	12	10	12	15	10	7
Montachia bit shift or multitable membra montachia bit shift or		Pulse techniques					113	146	124	137	157	187	\sim	\searrow	5	3	3	3	6	5
Monotable, productivale or multivale options of internal, external positive in referenal, external positive in referenal positive in reference in			Monostable, bistable or multistable		Bistable circuits		686	660	764	681	893	860	~		11	6	8	10	10	11
Statish or multistable suntriving desices Statish or multistab					Astable circuits		260	291	303	318	393	370	1	_	3	2	2	2	1	1
Statistic of uniformalization principal growth or the principal of connecting (disconnecting of connecting of co			circuits		Bistable circuits		240	240	257	339	426	421		$\overline{\wedge}$	4	7	7	5	5	4
Semiconductor devices Semi						1	2382	2477	_	2229	_	_	$\overline{}$	/	0	0	0	0	0	40
Semiconductor devices Semiconductor bodies Semiconductor devices with white the implication Semiconductor devices Semiconductor			devices Connecting/disconnecting	-			-	-	-	_	_		_	$\overline{}$	-	-	-			
Parameter Para				-					1000					~ \	8	-	6	14	10	4
Micronection layout Micronectic layout Micronection layout		Semiconductor devices	transition, e.g. field effect		1			-	-				\sim		0	0	0	0	0	
Static Memory Static Memory Security			and insulating layers	Interconnection layout			-	_	_	_	_	_	\angle	~~/	5	6	2	5	3	_
Reading and writing of data to an inemory			state devices components formed		,		41561	42679	45547	46776	50766	52926	/	~/	12	19	11	14	15	33
Selecting address in memory Static Memory Selecting address in Selecting				Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down			648	679	771	804	830	898	/	\wedge	8	11	23	29	17	20
Static Memory Static Memory			memory	Read-write (R-W) timing or clocking			1236	1186	1391	1311	1280	1392	5	\wedge	7	7	22	29	17	16
Static Memory Mark Material Responsibles Mark Mestatance random access Mark Mestatance			Selecting address in memory		1		602	651	614	567	589	593	1	$\langle \wedge \rangle$	13	7	14	21	13	10
Material Resistance random access Institute Material Resistance		Static Memory		Comprising metal oxide memory	1		963	_	938	893	719	665	~	/	0	0	0	0	2	53
Memory elements Minter of sing amming circuits or methods Mi		•	w/ RRAM Resistance random access	Reading or sensing circuits or			531	633	853	907	1039	1024	\rightarrow		0	0	0	0	1	50
Wireless networks			memory elements	methods Writing or programming circuits or			_	_	_		_	_	_	-	0	0	0	0	2	60
Adaptive coding Motion compensation Video coding, decoding Transform coding Joy Memory arrangements Wireless networks Network topologies Access security Authentication Access security Authentication Piss a 1188 1188 1188 1188 1188 1188 1188			4	methods	J		-	_	_		_	_	(~	_/		0		-	4	00
Motion compensation				-										/ V	25	32		60		
Video coding, decoding by Memory arrangements									-			-	/	~^	6	3	10	11		16
Description			Motion compensation				4211	4671	4965	5406	5486	5437		_	0	1	2	2	10	9
Wireless networks		Video coding, decoding	Transform coding				6684	6602	5898	5706	5793	5675	1	$\nearrow \land$	1	3	6	3	7	2
Authentication Auth							1860	1679	1309	1256	1333	1271	1	5	4	2	2	4	8	7
Communication services Communication services Communication services Communication services Communication services M2M, MTC 1179 2213 3358 4376 5963 6912 0 0 1 1 10 12 25 16 17 17 17 17 17 17 18 18			w/ Parallelised computational	1			892	909	1021	1039	1182	1286	7	\	6	3	1	3	5	7
M2M, MTC 1179 213 3158 4576 5963 6912 0 0 1 10 22 26			arrangements	Collecting sensor information]		-	_	_		_	_	_		0	0	0	5	11	4
Nr.C. RFD 1173 2516 4425 7084 10051 1179 0 0 0 1 1 11 1 19 16								_	_		_	-			0	-	,	10		26
Subscription-based services 687 888 1272 1375 1602 1486 0 0 1 4 11 3			Communication services												-	,		20	-	20
Wireless networks Self-organising networks 6355 6806 6942 7049 7890 8313 0 2 1 5 7 6 Access security Authentication 2735 3325 4063 4594 5808 6152 0 1 1 8 16 9 Security Authentication 5794 6371 7932 8529 10637 1301 2 4 5 12 37 19													_		U	0	1	11		16
Network topologies Self-organising networks 6195 6806 6942 7049 7890 8313 0 2 1 5 7 6		Wireless networks		Subscription-based services			_	-	_	_	_	-	/		0	0	1	4	11	3
Security Authentication 5794 6371 7932 8929 10657 11301 / 2 4 5 12 37 19										1	I	1			I-	1	I.	I-	7	6
		Wireless networks	Network topologies	Self-organising networks			6195	6806	6942	7049	/890	8313	_	~	0	2	1	5	,	_
		Wireless networks	Network topologies				-	0000	0342	,,,,,	,,,,,,	_	$\overline{}$		0	1	1	8	16	9
		Wireless networks		Access security			2735	3325	4063	4924	5808	6152	_	~/ ^ 	0	1 4	1 5	8		9



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